CLAIMS

Please amend the claims as follows:

1. (currently amended) A data processing system, comprising:

one or more processing cores; and

a memory controller, coupled to said one or more processing cores, that controls access to a system memory containing a plurality of rows, said memory controller having an access history mechanism ~~memory speculation table~~ that ~~stores~~ maintains historical information regarding prior memory accesses, wherein said memory controller ~~includes: means~~, responsive to a memory access request, ~~for directing~~ directs an access to a selected row among the plurality of rows in the system memory to service the memory access request; and ~~means for~~ speculatively ~~causing~~ causes the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism ~~in said memory speculation table~~.

2. (original) The data processing system of Claim 1, wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip.

3. (currently amended) The data processing system of Claim 1, wherein said access history mechanism ~~memory speculation table stores~~ maintains a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

4. (currently amended) The data processing system of Claim 1, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said ~~memory speculation table~~ access history mechanism stores said historical information on a per-bank basis.

5. (currently amended) The data processing system of Claim 1, wherein said plurality of rows are organized in one or more banks, and wherein said ~~means for~~ memory controller speculatively ~~continuing~~ continues to energize said Row Address Strobe for said selected row ~~comprises means for speculatively continuing to energize said selected row~~ until a next access to another row within a same bank as said selected row.

6. (currently amended) The data processing system of Claim 1, wherein:

said system memory comprises a first system memory;

said memory controller comprises a first memory controller;

said data processing system further comprising ~~a second system memory and~~ a second memory controller that controls access to ~~the~~ a second system memory; and

said means for speculatively continuing to energize said selected row comprises means for speculatively continuing to energize said Row Address Strobe for said selected row based upon historical information recorded by said second memory controller.

7. (currently amended) The data processing system of Claim 1, wherein said plurality of rows are organized in one or more banks, and wherein said data processing system further comprises ~~comprising~~:

a system interconnect coupling said plurality of processing cores; and

one or more cache hierarchies coupled to said plurality of processing cores that cache data from said system memory, wherein said one or more cache memories communicate historical bank access information to said memory controller.

8. (currently amended) A memory controller for controlling a system memory of a data processing system, wherein the system memory includes a plurality of rows, said memory controller comprising:

~~a memory speculation table~~ an access history mechanism that ~~stores~~ maintains historical information regarding prior memory accesses; and

~~means~~ a state machine that, responsive to a memory access request, ~~for directing~~ directs an access to a selected row among the plurality of rows in the system memory to service the memory access request[[;]] and ~~means for~~ speculatively ~~causing~~ causes the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism ~~memory speculation table~~.

9. (currently amended) The memory controller of Claim 8, wherein said access history mechanism ~~memory speculation table stores~~ maintains a respective memory access history for each of a plurality of threads executing within said data processing system.

10. (currently amended) The memory controller of Claim 8, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said ~~memory speculation table~~ access history mechanism stores said historical information on a per-bank basis.

11. (currently amended) The memory controller of Claim 8, wherein said plurality of rows are organized in one or more banks, and wherein said state machine ~~means for speculatively continuing to energize said selected row comprises means for~~ causes said system memory to speculatively ~~continuing~~ continue to energize said Row Address Strobe for said selected row until a next access to another row within a same bank as said selected row.

12. (currently amended) The memory controller of Claim 8, wherein:

said state machine ~~means for speculatively continuing to energize said selected row comprises means for~~ causes said system memory to speculatively continue ~~continuing~~ to energize said Row Address Strobe for said selected row based upon historical information maintained ~~recorded~~ by another memory controller.

13. (currently amended) A method of operating a memory controller of a system memory of a data processing system, wherein the system memory contains a plurality of rows, said method comprising:

said memory controller ~~storing~~ maintaining historical information regarding prior memory accesses with an access history mechanism ~~in a memory speculation table~~;

in response to receipt of a memory access request, directing an access to a selected row among the plurality of rows in the system memory to service the memory access request; and

speculatively directing the system memory to continue to energize a Row Address Strobe for said selected row following said access based upon said historical information indicated by said access history mechanism ~~memory speculation table~~.

14. (currently amended) The method of Claim 13, wherein said ~~storing~~ maintaining comprises ~~storing~~ maintaining a respective memory access history for each of a plurality of threads executing within said data processing system.

15. (currently amended) The method of Claim 13, wherein said plurality of rows in said system memory are arranged in a plurality of banks, and wherein said ~~storing~~ maintaining comprises ~~storing~~ maintaining said historical information ~~in~~ of said access history mechanism ~~memory speculation table~~ on a per-bank basis.

16. (currently amended) The method of Claim 13, wherein said plurality of rows are organized in one or more banks, and wherein said step of speculatively continuing to energize said selected row comprises speculatively continuing to energize said Row Address Strobe for said selected row until a next access to another row within a same bank as said selected row.

17. (currently amended) The method of Claim 13, wherein said step of speculatively continuing to energize said selected row comprises speculatively continuing to energize said Row Address Strobe for said selected row based upon historical information recorded by another memory controller.

18. (new) The data processing system of Claim 1, wherein said access history mechanism comprises one or more state machines each having a plurality of different states, wherein each of said plurality of different states represents a prediction regarding whether the system memory should continue to energize a Row Address Strobe of said selected row of said system memory following an access.

19. (new) The memory controller of Claim 8, wherein said access history mechanism comprises one or more state machines each having a plurality of different states, wherein each of said plurality of different states represents a prediction regarding whether the system memory should continue to energize a Row Address Strobe of said selected row of said system memory following an access.

20. (new) The method of Claim 13, wherein said maintaining comprises maintaining one or more state machines each having a plurality of different states, wherein each of said plurality of different states represents a prediction regarding whether the system memory should continue to energize a Row Address Strobe of said selected row of said system memory following an access.